Accutron Inc.

ICT TEST, FIXTURE AND PROGRAMMING REQUIREMENTS

ICT Test, Fixture & Programming Requirements

 This bulletin is intended to provide general information on In-Circuit Test (ICT) and to document a basic set of requirements that need to be met in an effort to facilitate the production of an In-Circuit Test fixture and program for a given PCBA.

Included are sections on assumptions made when providing ICT quotations, Test Program coverage and content, Material and Documentation needed to provide and ICT fixture/program, a limited glossary of terms related to ICT and a section on Data and File Formats and transfer.

Portions of these guidelines are excerpted from documentation published by Teradyne Inc. and TTI Testron and are copyrighted by them.

I.   ASSUMPTIONS AND GUIDELINES

Due to the custom nature of individual test fixtures and programs, quotations are estimates of typical costs and schedules based on the information provided to us. Additional costs may be incurred if the information and materials provided are insufficient or inaccurate. Accordingly, any quotation is for budgetary purposes only.

The following assumptions and guidelines should be used during the design and layout of the circuit board as well as when requesting an ICT quotation. This will allow consideration to be made for all items that may affect testability and fixture/programming costs. See TB001 Designing for Testability Guidelines for more in-depth information.

A.   Mechanical

1.   All via holes and unused component locations should be solderable. Unsoldered holes require mechanical hold down or Iso-vac fixtures, which increase the fixture cost.

2.   All test pads and vias should be able to be probed using standard .100" probes. Additional charges must be made to accommodate .050" probes. Minimum test pad and test via spacing should be .050" on center. Additional fixture cost savings can be realized if minimum spacing is increased to .085". Dual-sided access should be avoided if at all possible due to increased fixture cost and complexity; increased difficulty in program debugging and physical fixture alignment generally result from this type of fixture.

3.   All signal nets should accessible from the solder side of the board. SMT to SMT only traces on the top side of the board should have a via added to the solder side. Solder side SMT to SMT traces should have a test pad added.

4.   Test pads should be made .035" - .040" (square if possible). They should be entered in the board netlist as a one pin component, and in the drill file (must have coordinates). Test pads of .025" are feasible, but increases the risk of mis-probes due to DUT tolerances.

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5.   All test pads and vias to be used as probe points must be free of soldermask, silkscreen, etc.

6.   A minimum of two tooling holes should be placed on the PCB, preferably on diagonally opposite corners.

7.   Tooling holes should be .125" +.003/-.000 or larger and placed .250" to .500" from the edges of the PCB.

8.   Tooling holes should be unplated.

9.   Adequate clearance is provided on all edges of the PCB to allow vacuum sealing.

10.   If possible, no components should extend from the solder side of the PCB more than .250". Taller components may require special fixture considerations.

B.   Electrical

1.   Multiple access points should be provided for all power and ground trace pairs.

2.   Each component should be considered separately. Neighboring components should be able to be isolated by disabling.

3.   Where possible, test functions should be provided in mask programmable parts to find open pins. Use otherwise unused pins to provide test functions.

4.   Use pull-up and pull-down resistors (100 ohms or greater) on output enables to allow testing each part or group of parts separately.

5.   Provide clock, oscillator, reset, read, write and enable inputs for test at typically slow test speeds. Clock and oscillator inputs should be able to be controlled by the tester.

6.   For LSI and micro-controllers, do not tie any external instruction access pins directly to power or ground. Use pull-up or pull-down resistors.

7.   Use sockets for parts that are free running and not able to stop or tri-state to allow testing of other parts on the bus.

8.   Avoid RC circuits directly connected to IC's. Put behind a 100 ohm resistor or use a TTL gate or a jumper to allow the ICT tester to drive control signals for testing.

C.   Checklist for Electrical Designer

1.   Is there individual control over tri-state component outputs?

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2.   Can ATE disable clocks?

3.   Can ATE insert an external clock?

4.   Are IC control signals controllable by ATE?

5.   Do PAL's have a disable or tri-state word or pin?

6.   Do PROM's have locations set aside for all one's and all zeros?

7.   Are pull-ups used on open collector outputs?

8.   Can feedback loops be opened by ATE?

D.   Checklist for Printed Circuit Board Designer

1.   Do all electrical PCB nodes have at least one probe target?

2.   Do power busses (plus and minus) have multiple probe targets?

3.   Is there at least one probe target per three digital devices on the PCB for ground wires?

4.   Are the probe targets solder covered?

5.   Are the probe targets at least .025" diameter (.035"-.040" preferred)?

6.   Is the minimum distance between any component edge and any probe target center .100"?

7.   Is the center-to-center distance between probe targets .100"?

8.   Are probe targets evenly distributed across the surface of the PCB?

9.   Are there two dedicated tooling holes on diagonally opposite corners of the PCB?

10.   Are the tooling holes at least .125" +.003"/-.000"?

11.   Is the tolerance between tooling holes ±.002"?

12.   Is the tolerance from PCB datum to probe targets ±.002"?

13.   Is the tolerance between the UUT datum and tooling holes ±.002"?

14.   Are the tooling holes unplated?

15.   Is there a .125" area free of components and test pads around the tooling holes?

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II.   ICT TEST COVERAGE AND METHODOLOGY

Testability as used in this document is defined as allowing 100% access to all circuit nodes (preferably from one side of the PCB). This includes access to unused component pins, component isolation (pull-ups), and soft grounds for IC control logic (clear, set, reset, enable, etc.). All attempts will be made to test the entire board. However certain devices and circuits (parallel paths which cannot be guarded, etc.) may not be tested. Untested devices or circuit configurations will be noted in the program. Limited tests, if any, will be flagged in the body of the program by attaching "LT" to the test title.

A.   TEST PROGRAM CONTENT

Typical ICT programs will include the following four main sections:

- ♦ shorts testing
- ♦ analog power-off testing
- ♦ power supply switching
- ♦ power-on testing

1.   SHORTS AND CONTINUITIES TEST SECTION

a)   SHORTS

100% of all detectable shorts between accessible nodes with a resistance of five (5) ohms or less. Devices that cause a short or appear to be a short (the normally closed contacts of a switch, small inductors, or potentiometers) are also tested in this section.

b)   CONTINUITIES

An unnamed (on schematic) but expected resistance of less than 5 ohms nominal between two nodes. Continuity checks are made for orientation of switches and relays. The continuity of long traces can also be checked if desirable.

c)   JUMPERS

A named (on schematic) but expected resistance of less than 5 ohms nominal between two nodes. This includes added wires and shunts.

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2.   ANALOG POWER-OFF TEST SECTION

Analog components are tested in this section without power applied to the board-under-test.

a)   RESISTORS

Resistors from 5 ohms to 100 megohms (including potentiometers) are verified to their value and tolerance plus system tolerances. Values less than 5 ohms are attempted as a continuity utilizing standard 3-wire techniques, and for value with 6-wire tests if desired. Note that 6-wire tests are an additional cost to fixture and program.

b)   CAPACITORS

All testable capacitors from 100pF to 999uF verified to their tolerance plus system tolerances. Parallel capacitors receive limited testing using "lump sum" calculations. Capacitors having parallel resistance where the X_c of the capacitor is approximately 3 times the resistance are not usually testable. Capacitors less than 100pF will be attempted using standard test methods but may not be measured depending upon circuit configuration.

c)   INDUCTORS AND TRANSFORMERS

Measured as an inductance test. If outside the range of the tester, then tested for continuity.

d)   DIODES

Measured for forward voltage drop and reverse leakage (Zeners to 110 Volts tested for breakdown).

e)   TRANSISTORS

Both junctions test as diodes. 6-wire saturation tests can usually be written if ordered.

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f)   **SPECIAL CIRCUIT CONFIGURATIONS**

A PCBA's circuit configuration can interfere with a tester's ability to test and report accurate component values. For example, circuits in parallel (resistor-capacitor, resistor-diode) or paths which include ICs may be unguardable. Such a situation requires bulk measurement of the parallel combination instead of individual component measurement. For most in-circuit tests, guards are set for isolation. If, however, the guard ration (the ratio of guard current to measured current) exceeds 10 (a rare occurrence), the resolution is affected. Parallel bus capacitors, parallel capacitor-resistor combinations, and parallel resistor-transistor junctions most commonly prevent high accuracy measurement of their components, for example.

3.   **POWER-ON TEST SECTION**

This section turns on and applies power, then tests all powered devices following these guidelines:

a)   **VOLTAGE**

0-99 Vdc or peak ac, plus 20% over-range. Tests are aborted if improper voltages are detected.

b)   **LINEAR COMPONENTS**

All testable discrete active components having Zehntel templates will be tested using that template. Op amps will be tested for full-scale output swing; regulators will be functionally tested to verify their output voltage.

c)   **DIGITAL DEVICES**

All DTL, TTL, CMOS, SSI and MSI devices in current Zehntel library will be tested to the component truth table using binary pattern generation (Gray Code stimuli) and signature analysis techniques. Where possible, LSI devices are given an inspection test to exercise some functions. Such testing verifies that the correct device is installed, properly oriented, and functional.

RAM/ROM is also tested using Gray code stimuli, which allows every address to be generated and every cell to be checked.

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III.   DOCUMENTATION AND MATERIAL REQUIREMENTS

Below is a list of the materials that we would like to have supplied to create an ICT fixture and program. Note that some information may not be an absolute requirement as various workarounds exist. However, the more data supplied in the required format, the more efficiently the process can move forward.

When supplying data for ICT it is preferable to have as much data as possible in machine-readable file format. This not only reduces some of the time required to produce the fixture/program, but also reduces the chances for error as well.

A.   GERBER FILES

Most drill and net information for the fixture can be extracted from GERBER files. Information on aperture D-Codes must be included. This is generally a separate ASCII file. Note that if supplying RS-274X data the D-Codes are included in the file header.

B.   NET OR NODE LISTING

Net list should show each part and pin number for each board trace (electrical net).

C.   DRILL FILE

This is an ASCII format file, which should also include tooling holes and SMT test pads. Most fixture manufacturers can also work with an ASCII drill tape. If necessary a drill plot can be digitized from a 1:1 mylar of the PCB.

D.   CURRENT REVISION FAB DRAWING

This should include the tooling hole locations.

E.   CAD OUTPUT FILE

See the File Format section for details on the needed format.

F.   CURRENT REVISION ASSEMBLY DRAWING

This should include all assembly details for both sides of the PCB.

G.   CURRENT BILL-OF-MATERIALS (BOM)

H.   CURRENT REVISION SCHEMATIC DRAWING

I.   ALL APPLICABLE ECOS

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J.   **LOADED FUNCTIONAL PCBA**

For fixture sealing the PCBA can be non-functional (but complete). In order to aid in fixture/program debug, a fully functional unit is preferred. Note that for final fixture/program acceptance a minimum of 5-10 units is desired. This can normally be accomplished by using part of the initial production run for this purpose.

K.   **COMPONENT DATA SHEETS**

Copies of the manufacturer's data sheets for components other than standard logic types. This is especially true of components not widely used such as unique interface chips, etc. We can generally determine what may be needed from the BOM. This should also include any equations for PALs, PLAs, test vectors, etc.

L.   **BARE PCB**

Used to learn low-impedance paths and other continuities, which may interfere with shorts testing as well as in debugging both the ICT fixture and program.

IV.   **GLOSSARY OF TERMS**

1:1 STABLE MYLAR ARTWORK

1:1 stable Mylar artwork is a scale copy of the PCB artwork (both sides, or in the case of multi-layer boards, all layers) reproduced on clear acetate Mylar for dimensional stability. Artwork must be positive and stable.

- *Positive* means the traces of the PCB are clearly indicated with a clear background as in a photo. (Negative versions cannot be used.)

- *Stable* indicates that the medium on which the artwork resides will not change dimensions with time or environmental conditions.

The artwork is used to digitize the drill pattern to create a padmaster drill tape.

** NOTE **

- If artwork is 2:1, it cannot be reduced; therefore, it is not considered stable.

- Paper artwork or blue line artwork cannot be substituted for clear acetate mylar.

- If only unstable artwork is available, the bare PCB is required for creating the drilling pattern. (This assumes that no CAD or drill information is available.)

APERTURE LISTING

A listing of pad sizes used in the Gerber files.

ASSEMBLY DRAWING (COMPONENT)

An assembly drawing depicts the physical location of all components on an assembled PCB, and the designation (type, part number) of each component. The assembly drawing is essential for the creation of the input list.

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** *NOTE* **

When a load PCB is not available, the component assembly drawing gives a clear picture of the PCB by indicating the sizes of components and whether any obstacles exist on the board.

BARE PRINTED CIRCUIT BOARD

The bare printed circuit board is a PCB after it has been drilled and etched, but before the components have been installed or the solder applied. This board is used to verify the fixture and is probed electrically to verify active nodes. The bare board is often used to create the drill tape. It acts as a drill guide when artwork is not supplied or is questionable, and also serves as the template for making the clear and shorting plates.

** *WARNING* **

The error rate increases when drilling must be done from a bare board, as tolerances may vary from PCB to PCB.

FABRICATION DRAWING (MECHANICAL)

A fabrication drawing specifies the contour of a PCB, the location and size of tooling holes, and the sizes of other holes in the board. This drawing determines tooling hole locations and sizes.

The fab drawing is also used to verify dimensions between Mylar and boards.

FULL PINS NET LISTING

A general data list that contains the parts designator, the value or generic part name, the pin number, the type of pin, the net name, and the X-Y positional information to the I/O pin. This file can then be reconstructed to provide the drill tape, test pin location (nodal), fixture wiring lists, and the program input lists.

GERBER FILES

Photo plotting files of the PCB showing all traces, pads, flashes and draws required to build the PCB. Drill and Net information can be extracted from Gerber files if available.

INPUT LIST

A program file which contains information for each component to be tested on the PCB. This file consists of the part designator, value, tolerances, and the node number that has been assigned to each device pin. This list is the input data for the program generator.

ISOLATED NODE

A node or test point located on an unused component lead. Typically, an isolated node occurs when there is an unused gate on a multi-gate IC. Often these nodes do not appear on a schematic drawing or a net list but are found on the inner layer Mylar artwork. It is often desirable to provide isolated nodes with test points in anticipation of future design changes.

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LOADED PRINTED CIRCUIT BOARD

Often referred to as a stuffed or functional PCB, this board has all components inserted and soldered in place. Certain ancillary components, such as card ejectors, may be omitted if they are not in place during testing. The loaded PCB is critical to the construction of the fixture and is required to ensure a proper top seal.

A known-good loaded board is essential for program debug. The more boards available the better the quality and coverage of the initial test program.

NET LIST

A listing of all "electrical" nets found on a PCB. (A net is equivalent to a "node" or PC trace.) A jumper from one trace to another connects two nets. The total quantity of nets provides the number of active nodes that must be probed in the fixture.

PADMASTER

A 1:1 Mylar showing the location of all component holes, feed-throughs, and traces.

PARTS LIST (BOM)

A list describing the components used on a particular PCB assembly. Usually it contains a part number, a circuit designator (e.g., R12, C13), and a description of the type, value, and tolerance (if appropriate); for example, 47K, 10%, 1/4w. The parts list must list the commercial name of any IC of other device. The parts list is essential in the creation of the input list and is critical to program development. The parts list acts as the basic specification for the input list and thus the test program.

POWER-ON SEQUENCE

A sequence of commands in the test program which causes test system power supply voltages to be applied to the PCB under test. This voltage allows active components to be tested with power applied to the board. A power-on sequence includes a test for application of correct voltages before proceeding further with the test.

SCHEMATIC

A drawing depicting the various components on the PCB and their electrical interconnections. This schematic is critical, and required for program development. A fixture's active nodes are marked and numbered on the noded schematic.

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V.   FILE FORMATS AND MEDIA

A.   INTRODUCTION

Drill data can be provided as XY listings or through a CAD file. If a CAD file is supplied, it can be used both for drilling purposes and for fixture wire listings and documentation. Drill XY data may be supplied on a paper tape in ASCII or EIA format (XY listings only). Drill and CAD data may be supplied on magnetic media or via modem transfer with arrangements made in advance.

B. XY FILES

There are several common XY formats that can be used. It is important that the drill file contain leading zeros, since the assumed decimal place is two numeric digits from the left. Trailing zeros may be omitted.

C. CAD FILES

For fixturing purposes CAD files should contain the component name, pin number, XY location and the Net name. These files eliminate the need for ohming out analog points to determine pin 1, and searching a board or layout for components or test pads and vias. An example CAD format is listed below. Column structure of the file is not critical. It is more important that all the necessary information be included.

CAD OUTPUT FORMAT EXAMPLE

Component Name	Pin Number	X Location	Y Location	Net Name
U1	1	X-3.620	Y4.251	NET001

D. MAGNETIC MEDIA FORMATS

Data files should be supplied in MS-DOS format on 3.5" diskettes.

E. TELECOMMUNICATIONS

Data files may be emailed to: sales@accutroninc.com

Files compressed into a single archive volume using ZIP format are preferred to reduce data transmission time.

With previous arrangements, we can accept data files via modem.